IN THE CLAIMS

The following Listing of Claims will replace all prior versions and listings of the claims.

Listing of Claims:

1. (Currently Amended) A channel adapter comprising:

a host interface, the host interface operatively connected to a memory by a local bus, the memory containing at least one completion queue and at least one event queue;

a link interface, the link interface operatively connected to a network;

a packet processing engine, the packet processing engine moving data between the host interface and the link interface;

a completion queue engine, the completion queue engine processing completion requests from the packet processing engine by writing the appropriate at least one of the at least one completion queue and at least one event queue;

an address translation engine, the address translation engine translating a virtual address into a physical address of a translation protection table in the memory, the address translation engine comprises an inbound request processor and a request completion processor, the inbound request processor receiving a request for address translation of the virtual address, the request completion processor sending the physical address of the memory associated with the virtual address and retrieved from the translation protection table to at least one of the packet processing engine and the completion queue engine in response to the request ; and

~~a completion queue engine, the completion queue engine processing completion requests from the packet processing engine by writing the appropriate at least one of the at least one completion queue and at least one event queue,~~

wherein the packet processing engine is not impacted by any address translation functionality, completion queue accesses, or event queue accesses thereby significantly enhancing the performance of [[a]] the channel adapter.

2.-16. (Cancelled).

17. (Currently amended) The adapter according to claim [[16]] 1, wherein the inbound request processor comprises:

at least one switching device, the at least one switching device receiving the request for address translation from at least one of the packet processing engine, the completion queue engine, and the request completion processor;

at least one request register bank, each at least one request register bank comprising a request register, and a data register, the request register storing the request, the data register storing data received from at least one of the packet processing engine, the completion queue engine, and the request completion processor related to the request;

arbitration logic, the arbitration logic selecting between all outstanding requests and outputting a protection index of one of the requests, the arbitration logic associating a tag value with each request;

a local bus interface, the local bus interface receiving the protection index, checking whether the protection index is out of bounds, and adding the protection index with a base address of the translation protection table generating the physical address to the translation protection table; and

a request processor, the request processor sending errors related to the request to the request completion processor, the request processor sending a request and the physical address to the host interface to read the translation protection table.

18. (Original) The adapter according to claim 17, wherein the local bus interface comprises a size register and at least one base address register, the size register and at least one base address register being programmable over the local bus by at least one of the operating system and the application, the contents of the size register being compared to the protection index to determine whether the protection index is out of bounds, the base address register containing the base address of the translation protection table.

19. (Original) The adapter according to claim 17, wherein the data stored by the data register comprises one of a virtual address, a key, the protection index, and a protection domain.

20. (Currently amended) The adapter according to claim [[16]] 1, wherein the request completion processor comprises a decoder, at least one set of receive data buffers, arbitration logic, at least one staging register, permission checking logic, protection index calculation logic, and bounds checking logic.

21. (Original) The adapter according to claim 20, wherein each at least one set of receive data buffers comprises a read complete register and at least one data buffer, the read complete register signaling a request to the arbitration logic once all at least one data buffer for the set have been filled.

22. (Original) The adapter according to claim 20, wherein the decoder, at least one set of receive data buffers, and arbitration logic operate at a different clock speed than the at least one staging register, permission checking logic, protection index calculation logic, and bounds checking logic.

23. (Original) The adapter according to claim 19, further comprising a first valid register associated with the permission checking logic, a second valid register associated with the protection index calculation logic, and a third valid register associated with the bounds checking logic, each valid register containing an indication that the processing for the associated logic may begin.

24. – 44. (Cancelled).

45. (Currently amended) A computing device with enhanced channel adapter performance comprising:

a memory, the memory containing at least one translation protection table, at least one completion queue, at least one event queue, and at least one of a data buffer and a one work queue; and

a channel adapter, the channel adapter comprising:

a packet processing engine, the packet processing engine moving data between a first interface and a second interface;

a completion queue engine, the completion queue engine processing completion requests from the packet processing engine by writing the appropriate at least one of the at least one completion queue and the at least one event queue;

an address translation engine, the address translation engine translating a virtual address into a physical address of the at least one translation protection table in the memory, the address translation engine comprises an inbound request processor and a request completion processor, the inbound request processor receiving a request for address translation of the virtual address, the request completion processor sending the physical address of the memory associated with the virtual address and retrieved from the translation protection table to at least one of the packet processing engine and the completion queue engine in response to the request; ~~and~~

~~a completion queue engine, the completion queue engine processing completion requests from the packet processing engine by writing the appropriate at least one of the at least one completion queue and the at least one event queue~~, and

wherein the packet processing engine is not impacted by any address translation functionality, completion queue accesses, or event queue accesses thereby significantly enhancing the performance of the channel adapter.

46. (Original) The device according to claim 45, wherein the first interface comprises a host interface, the host interface operatively connected between the channel adapter and the memory by a local bus.

47. (Cancelled).

48. (Original) The device according to claim 45, wherein the second interface comprises a link interface, the link interface operatively connected between the channel adapter and a network.

49. (Cancelled).